REMARKS

Claims 1-23 and 25-32 are pending in this application. Claims 1, 11, 14, 22, 23 and 26-27 are amended herein. Claim 24 has been canceled. Claims 28-32 have been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claim 14, which was objected to because of an informality, has been amended as suggested by the Examiner.

Each of the originally filed claims has been rejected in view of prior art. In particular, claims 1-10, 22, 23 and 26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Bogin (U.S. Patent No. 6,584,526) and claims 11-22, 24, 25 and 27 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Borkar et al. (U.S. Patent No. 6,538,584). Applicant respectfully traverses this rejection.

Each of the independent claims has been amended in a way that clearly distinguished from the prior art. No new matter is added by these amendments.

The following discussion of Bogin will show that same can only be considered as technical background for the present invention. Subsequently, reference will be made to the independent claim 1. These explanations equally apply to independent claims 22 and 26.

Bogin relates to an inserting bus inversion scheme in bus path without increased access latency (column 1, lines 18-30 of Bogin). The bus inversion system of Bogin comprises a first bus unit including a first conditional bus inverter to conditionally invert each of a plurality of bus signals from the first bus device to the bus. Therefore, the bus inversion system of Bogin is configured to invert each of the data bits if more than half of them are active. Thus, each bus line requires an additional inverter.

The subject of claim 1 of the present invention is novel compared to Bogin with regard to the following features:

- A means for examining the data word in order to determine whether a first number of bits of the data word with a first logical state or a second number of bits of the data word with a second logical state exceeds a predetermined threshold, the predetermined threshold being a value that is higher than 50% of the total number of bits of the data word,
- A means for changing the state of at least one bit of the data word ... , so that the first number of bits and the second number of bits of the encoded data word are below the predetermined threshold.

The following discussion will also show that these features are not rendered obvious by the bus inversion system disclosed by Bogin.

As it is known, in today's electronic systems, like for example in a computer system, especially the memory system and the linking structures, i.e., the data buses, over which the electronic devices communicate with the additional devices, e.g., memory devices, are of great importance as they determine the capacity of overall electronic systems to a high extent. An important performance feature of data buses hereby is the transmission rate with which the data signals are transmitted over the data buses between the communicating electronic devices. Here, the maximum transmission rate results from the bus clock frequency, the number of bus clocks per data transfer and the number of bytes transmitted per transfer corresponding to the bus width. An increase of performance of the data transmission via a data bus is therefore generally achieved by increasing the bus clock frequency or by an increase of the bus width.

According to the present invention, the inventive encoder contains a number of inverters which is thereby dependent on the bit width of the data word and therefore the width of the data bus is selected so that a sufficient number of signal data may be changed in order to effectively reduce and/or avoid the synchronous switching noise (SSN), i.e., by changing the signal data the simultaneous switching over of identical signal values is reduced in order to reduce internal supply voltage drops. It is for example possible to provide as many inverters that after an encoding there is always a ratio possible between the logical signal states ("0," or "1") of the data word of about 1:1, wherein for this at maximum one inverter is necessary for every second signal line.

Therefore, in order to limit the number of inverters, the present invention teaches to examine the data word in order to determine whether a first number of bits of the data word with a first logical state or a second number of bits of the data word with a second logical state exceeds a predetermined threshold, the predetermined threshold being a value that is higher than 50% of the total number of bits of the data word.

Based on the examination of the data word, the state of at least one bit of the data word from the number of bits exceeding the predetermined threshold is changed in order to create an encoded data word if the predetermined threshold is exceeded by the data word, so that the first number of bits and second number of bits of the encoded data word are below the predetermined threshold.

Therefore, the inventive encoder can be implemented with a reduced number of inverters so that the technical expense for the realization of a bus system having lowered synchronous switching noise (SSN) can be reduced.

It is clear from the above discussion that Bogin does not give a person skilled in the art any motivation to deviate from the teaching presented therein with respect to the arrangement of the data bus inversion system comprising an additional inverter for each bit line so that each of a plurality of bus signals can conditionally be inverted.

The following discussion of Borkar will show that same can only be considered as technical background for the present invention. Subsequently, reference will be made to claim 11, wherein the explanations equally apply to the parallel claims 22 and 27.

Borkar relates to a transition reduction encoder using current and last bit sets. The encoder according to Borkar involves a circuit including a first set of conductors to carry a current bit set and last bit set circuitry to hold and provide a last bit set. The circuit also includes a driver coupled to interconnect conductors to provide signals from the drivers to the interconnect conductors and an encoder to receive the last bit set and the current bit set and determine whether to provide the current bit set or an encoded version of the current bit set to the drivers. Therefore, the encoder according to Borkar requires an additional inverter for each bus line to be able to invert each of the data bits.

The subject matter of claim 11, and correspondingly that of claims 22 and 27, of the present invention is novel compared to Borkar with respect to the following features:

- a means for changing the state of at least one bit of the data word from the number of bits of the data word, due to which the predetermined threshold is exceeded, and at most 50% of the bits of the data word in order to create an encoded data word if the predetermined threshold is exceeded by the data word, so that the number of equal transitions between the two states of each bit of the encoded data word and the preceding data word is below the predetermined threshold.

The following discussion will show that these features are not rendered obvious by the transition reduction encoder using current and last bit sets disclosed by Borkar.

According to the present invention, the inventive encoder contains a number of inverters which is thereby dependent on the bit width of the data word and therefore the width of the data bus is selected so that a sufficient number of signal data may be changed in order to effectively reduce and/or avoid the synchronous switching noise SSN, wherein for this at maximum one inverter is necessary for every second signal line.

In order to limit the number of inverters, the present invention teaches to examine the data word by comparing the data word to a preceding data word in order to determine whether the number of equal transitions between the two states of each bit of the data word and the preceding data word exceeds a predetermined threshold, the predetermined threshold being chosen to ensure a secure transmission of the data word when the number is below the predetermined threshold.

Therefore, the inventive encoder can be implemented with a reduced number of inverters so that the technical expense for the realization of a bus system having a lowered synchronous switching noise (SSN) can be reduced.

It becomes clear that the subject matter of the newly submitted claims cannot be rendered obvious by the disclosure of Borkar.

Thus, the above discussion clearly shows that the encoding concept according to the present invention is neither anticipated nor rendered obvious by the prior art documents.

Thus, the reconsideration concerning the patentability of the claimed subject matter is respectfully requested.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

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